Analysis of Balanced Active Doubler for Broad-Band Operation—The Frequency-Tuning Concept

Belinda Piernas, Kenjiro Nishikawa, *Member, IEEE*, Tadao Nakagawa, *Member, IEEE*, Hitoshi Hayashi, *Member, IEEE*, and Katsuhiko Araki

***Abstract*—A comprehensive analysis of an active balanced frequency doubler is described and proposed as a new concept: tuning the center frequency at which the doubler exhibits its highest performance to extend the usable bandwidth of the device. The concept is validated using a fabricated V-band pseudomorphic high electron-mobility transistor frequency doubler. For this device, a substantial improvement in the usable bandwidth (more than double) is achieved, demonstrating that the proposed concept is particularly suitable for the realization of high spectral purity and widely tunable V-band frequency sources.**

***Index Terms*—Balanced frequency doubler, broad-band operation, circuit theory and design, 3-D MMIC technology.**

I. Introduction

THE increasing interest in millimeter-wave wireless communication systems, especially V-band frequency systems, raises the need for low cost, widely tunable, and high-quality millimeter-wave sources. Possible candidates are either the direct use of V-band oscillators [1], [2] or the use of lower frequency oscillators combined with frequency multipliers [3], [4]. The latter approach is more effective from the standpoint of phase-noise performance. However, the tight frequency band over which the doubler achieves proper fundamental-frequency rejection and isolation between the fundamental and the second harmonic limits the source bandwidth.

To achieve high spectral purity and broad-band operation, the active balanced doubler configuration is preferred because it provides efficient rejection of the fundamental and odd-harmonic frequencies. In this case, the bandwidth of the doubler is mainly limited by the phase and amplitude unbalance of the hybrid that increases with frequency. To overcome this limitation, we have previously reported an expanded bandwidth operation balanced doubler [5] that uses a novel rat-race hybrid [6] and is formed using three-dimensional (3-D) monolithic microwave integrated circuit (MMIC) technology [7].

To increase the usable bandwidth of the balanced active doubler even more, the authors propose the novel concept of frequency tuning. The concept, based on an asymmetry of the gate–source bias of the two transistors, enables the phase and amplitude unbalance of the hybrid to be locally offset, leading to a shift of the center frequency at which the highest spectral purity is achieved.

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The authors are with the NTT Network Innovation Laboratories, Kanagawa 239-0847, Japan.

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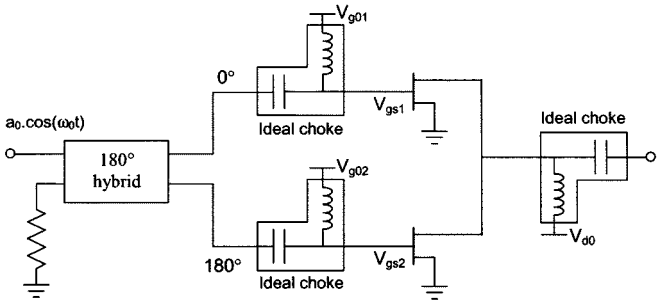

Fig. 1. Basic configuration of a balanced active doubler.

An analysis of balanced frequency-doubler operation and details of the frequency-tuning concept are presented. The proposed concept is experimentally validated using the fabricated V-band pseudomorphic high electron mobility transistor (pHEMT) frequency doubler reported in [5]. Local fundamental-frequency rejection as high as 40 dB is achieved for an input signal frequency varying from 26.7 to 37 GHz. Moreover, since the output power of the second harmonic is not strongly affected by the transistor bias unbalance, the isolation between the fundamental and second harmonic is also improved. Local isolation better than 30 dB is achieved from 26.9 to 36 GHz. With regard to previous measurements, the results indicate that the increase in the usable bandwidth of the doubler was over 100%.

II. Analysis of Balanced Active Doubler Operation

A. Mathematical Formulation

The basic configuration of the balanced frequency doubler considered in this analysis is shown in Fig. 1. It consists of two identical transistors and a 180° rat-race hybrid whose center frequency is f_c. For an input signal of frequency $f_0\,(\omega_0/2\pi)$ different from the center frequency, the hybrid exhibits amplitude unbalance $k(\omega_0)$ and a phase unbalance $\varphi(\omega_0)$ between its two outputs.

Let us assume that for each transistor, both of which are biased with constant drain–source voltage, the input-output relationship in the time domain can be expressed by a Taylor series [8], [11] and [12]

$$i(t) \cong A_0 + A_1 V_{\rm gs}(t) + A_2 V_{\rm gs}^2(t) + A_3 V_{\rm gs}^3(t) + \cdots \quad (1)$$

where $V_{\rm gs}(t)$ is the gate–source input voltage of each transistor containing dc and ac components.

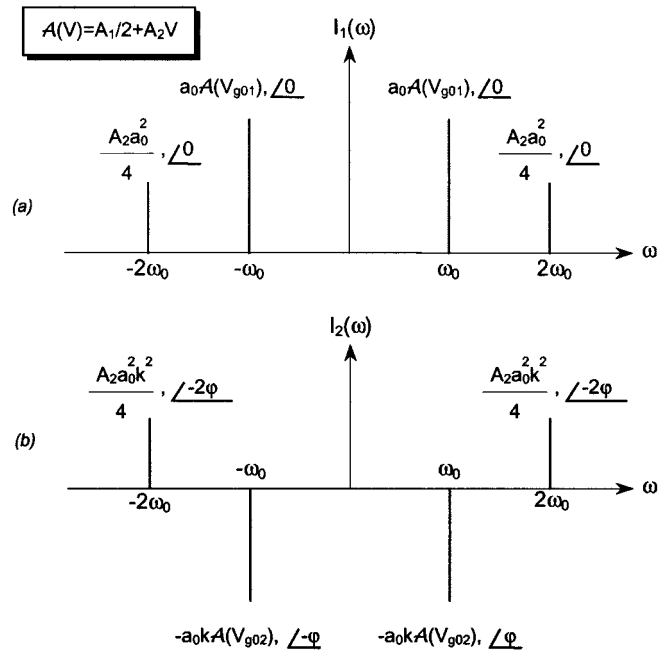

Fig. 2. Schematic representation of the output current spectrum. (a) I_1 and (b) I_2 of the frequency-doubler transistors.

Considering the hybrid characteristics, the input voltage of the transistors can be expressed as

$$\begin{aligned} V_{\mathrm{gs1}} &= V_{\mathrm{g01}} + a_0 \cos(\omega_0 t) \\ V_{\mathrm{gs2}} &= V_{\mathrm{g02}} + a_0 k(\omega_0) \cos\left(\omega_0 t + 180^\circ + \varphi(\omega_0)\right) \end{aligned} \tag{2}$$

where $f_0 = \omega_0/2\pi$ is the input signal frequency.

Combining (1) and (2) allows us to deduce the output current of each transistor. Up to the second order, it leads to

$$I_1(t) = a_0\left(A_1 + 2V_{\mathrm{g01}}A_2\right)\cos(\omega_0 t) + \frac{A_2 a_0^2}{2}\cos(2\omega_0 t) \tag{3}$$

$$\begin{aligned} I_2(t) = &- a_0 k(\omega_0)\left(A_1 + 2V_{\mathrm{g02}}A_2\right)\cos\left(\omega_0 t + \varphi(\omega_0)\right) \\ &+ \frac{A_2 a_0^2 k^2(\omega_0)}{2}\cos\left(2\omega_0 t + 2\varphi(\omega_0)\right). \end{aligned} \tag{4}$$

Note that the dc components eliminated in (3) and (4) for simplification will be suppressed at the circuit output by capacitance filtering.

The current spectrums (see Fig. 2) are deduced by Fourier transformation of (3) and (4) as follows:

$$\begin{aligned} I_1(\omega) = &\frac{a_0}{2}\left(A_1 + 2V_{\mathrm{g01}}A_2\right)\left[\delta(\omega_0) + \delta(-\omega_0)\right] \\ &+ \frac{A_2 a_0^2}{4}\left[\delta(2\omega_0) + \delta(-2\omega_0)\right] \end{aligned} \tag{5}$$

$$\begin{aligned} I_2(\omega) = &- \frac{a_0 k(\omega_0)}{2}\left(A_1 + 2V_{\mathrm{g02}}A_2\right) \\ &\cdot \left[\delta(\omega_0)\, e^{j\varphi(\omega_0)} + \delta(-\omega_0)\, e^{-j\varphi(\omega_0)}\right] \\ &+ \frac{A_2 a_0^2 k^2(\omega_0)}{4} \\ &\cdot \left[\delta(2\omega_0)\, e^{2j\varphi(\omega_0)} + \delta(-2\omega_0)\, e^{-2j\varphi(\omega_0)}\right]. \end{aligned} \tag{6}$$

The total output current spectrum $I_T(\omega)$ of the balanced active doubler can be directly deduced from combining (5) and (6) as follows:

$$\begin{aligned} I_T(\omega) &= a_0\left[\frac{A_1}{2}\left(1 - k e^{j\varphi}\right) + A_2\left(V_{\mathrm{g01}} - k V_{\mathrm{g02}} e^{j\varphi}\right)\right]\delta(\omega_0) \\ &+ a_0\left[\frac{A_1}{2}\left(1 - k e^{-j\varphi}\right) + A_2\left(V_{\mathrm{g01}} - k V_{\mathrm{g02}} e^{-j\varphi}\right)\right]\delta(-\omega_0) \\ &+ \frac{A_2 a_0^2}{4}\left[\left(1 + k^2 e^{2j\varphi}\right)\delta(2\omega_0) + \left(1 + k^2 e^{-2j\varphi}\right)\delta(-2\omega_0)\right]. \end{aligned} \tag{7}$$

Assuming the frequency doubler is terminated by load Z_L (typically $Z_L = 50\ \Omega$), the output power is proportional to the integral

$$P \propto \int_{-\infty}^{+\infty} |i_T(t)|^2\, dt = \int_{-\infty}^{+\infty} |I_T(\omega)|^2\, d\omega. \tag{8}$$

Combining (7) and (8), it is found that the output power of the fundamental frequency $f_0\,(\omega_0/2\pi)$ is proportional to

$$\begin{aligned} P^1(\omega_0) &\propto \frac{a_0^2 A_1^2}{2}\left[1 + k^2(\omega_0) - 2k(\omega_0)\cos\varphi(\omega_0)\right] \\ &+ 2a_0^2 A_2^2\left[V_{\mathrm{g01}}^2 - 2V_{\mathrm{g01}}V_{\mathrm{g02}}k(\omega_0)\cos\varphi(\omega_0) + k^2(\omega_0)\, V_{\mathrm{g02}}^2\right] \\ &+ 2a_0^2 A_1 A_2\left[V_{\mathrm{g01}} - \left(V_{\mathrm{g01}} + V_{\mathrm{g02}}\right)k(\omega_0)\cos\varphi(\omega_0)\right. \\ &\qquad \left. + k^2(\omega_0)\, V_{\mathrm{g02}}\right]. \end{aligned} \tag{9}$$

At the center frequency f_c, for which the hybrid is ideal ($\varphi(\omega_c) = 0$ and $k(\omega_c) = 1$), it is well known that the fundamental frequency is completely rejected ($P^1(\omega_c) = 0$) when the transistors are identically biased, i.e., $V_{\mathrm{g01}} = V_{\mathrm{g02}}$. Therefore, in a standard operation, the transistors are biased so that $V_{\mathrm{g01}} = V_{\mathrm{g02}} = V_{\mathrm{g0}}$. The output power of the fundamental frequency is then found to be

$$P^1(\omega_0) \propto P_{\mathrm{in}}(\omega_0)\, \mathcal{A}^2(V_{\mathrm{g0}})\left[1 + k^2(\omega_0) - 2k(\omega_0)\cos\varphi(\omega_0)\right] \tag{10}$$

where $P_{\mathrm{in}}(\omega_0) = 2a_0^2$ is the power input to the doubler and $\mathcal{A}(V_{\mathrm{g0}}) = A_1/2 + A_2 V_{\mathrm{g0}}$ is a constant depending from the transistors and their bias.

The fundamental-frequency rejection $S_0(\omega_0)$ defined as the ratio between the input power and the output power of the fundamental frequency can be expressed in decibels as

$$\begin{aligned} S_{0\mathrm{dB}}(\omega_0) &= -\mathcal{A}_{\mathrm{dB}} - 10\log\left[1 + k^2(\omega_0) - 2k(\omega_0)\cos\left(\varphi(\omega_0)\right)\right] \end{aligned} \tag{11}$$

where $\mathcal{A}_{\mathrm{dB}} = 20\log|\mathcal{A}|$.

In the same way, the output power of the second harmonic at $2f_0 = \omega_0/\pi$ can be deduced up to the second order from (7) and (8)

$$P^2(\omega_0) = \frac{P_{\max}^2(\omega_0)}{4}\left\{1 + k^4(\omega_0) + 2k^2(\omega_0)\cos\left(2\varphi(\omega_0)\right)\right\} \tag{12}$$

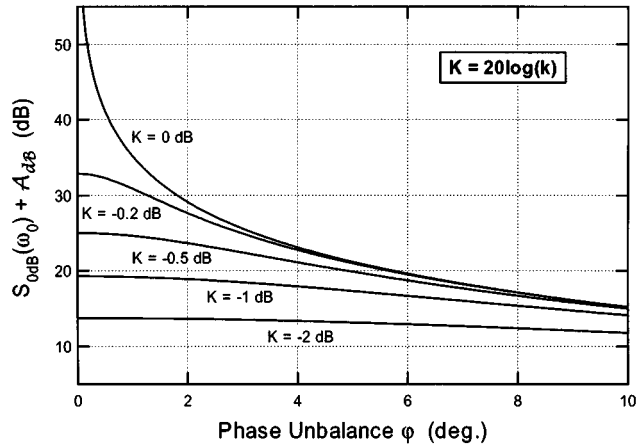

Fig. 3. Fundamental-frequency rejection evolution with phase and amplitude unbalance of the hybrid ($\mathcal{A}_{\rm dB} = {\rm cst}$).

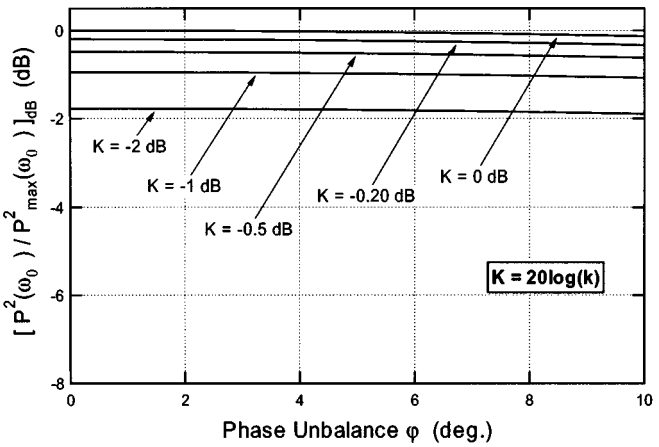

Fig. 4. Normalized output power of the second harmonic versus phase and amplitude unbalance of the hybrid.

where $P^2_{\rm max}(\omega_0) = a_0^4 A_2^2/2$ represents the maximum output power of the second harmonic.

Note that up to the second order, $P^2(\omega_0)$ is independent of $V_{\rm g0}$, the bias voltage of the transistors.

B. Simulated Results and Discussion

Fig. 3 shows that the fundamental-frequency rejection is highly dependent on the phase and amplitude unbalance of the hybrid. Infinite frequency rejection is achieved at $V_{\rm g01} = V_{\rm g02}$ when both amplitude and phase of the hybrid are balanced. If the hybrid exhibits no amplitude unbalance ($k \approx 1, K \approx 0\,{\rm dB}$), the fundamental-frequency rejection quickly decreases as the phase unbalance increases. As soon as amplitude unbalance is present, it dominates the phase unbalance.

As shown in Fig. 4, the output power of the second harmonic is maximum when both amplitude and phase of the hybrid are balanced. However, it is not strongly affected by the performance of the hybrid so its degradation with frequency is expected to be mainly due to input and output mismatching.

III. Concept of Frequency Tuning

A. Mathematical Formulation

As shown in Section II-B, the fundamental-frequency rejection of the doubler is strongly impacted by the performance of the hybrid. Thus, the bandwidth over which the doubler achieves high fundamental-frequency rejection (approximately 30 dB), is strongly limited around the center frequency of the hybrid.

In order to overcome this limitation and extend the usable bandwidth of the doubler, we propose the concept of frequency tuning. For a given frequency, this concept uses asymmetry in transistor bias voltage to offset the hybrid's defects.

Given the voltage difference $\Delta V = V_{\rm g01} - kV_{\rm g02}$ and assuming that one of the transistor gate–source voltages (e.g., $V_{\rm g02}$) is fixed and that $V_{\rm g01}$ is tuned, the output power of the fundamental frequency given by (9) can be rewritten as

$$\begin{aligned} P^1(\omega_0) &\propto \frac{a_0^2 A_1^2}{2}\left[1+k^2-2k\cos\varphi\right] \\ &\quad + 2a_0^2 A_2^2\left[\Delta V^2 + 2kV_{\rm g02}(\Delta V + kV_{\rm g02})\cdot(1-\cos\varphi)\right] \\ &\quad + 2a_0^2 A_1 A_2\left[(\Delta V + kV_{\rm g02})\cdot(1-k\cos\varphi)\right. \\ &\qquad \left. + kV_{\rm g02}\cdot(k-\cos\varphi)\right]. \end{aligned} \tag{13}$$

The derivation of (13) versus ΔV shows that a minimum in the output power of the fundamental frequency exists and is achieved when the voltage difference ΔV is equal to

$$\Delta V_0(\omega_0) = -kV_{\rm g02}(1-\cos\varphi) - \frac{A_1}{2A_2}(1-k\cos\varphi). \tag{14}$$

Combining (13) and (14), the minimum output power of the fundamental frequency $f_0 = \omega_0/2\pi$ can be expressed in terms of $k(\omega_0)$ and $\varphi(\omega_0)$ as

$$P^1_{\rm min}(\omega_0) \propto P_{\rm in}(\omega_0)\,\mathcal{A}^2(V_{\rm g02})\,k^2(\omega_0)\sin^2\left(\varphi(\omega_0)\right) \tag{15}$$

where $\mathcal{A}(V_{\rm g02}) = A_1/2 + A_2 V_{\rm g02}$ is the constant of the transistor, as defined in Section II-A.

Fundamental-frequency rejection $S_0(\omega_0)$ after bias compensation is then given by

$$S_{0\rm dB}(\omega_0) = -\mathcal{A}_{\rm dB} - 10\log\left[k^2(\omega_0)\sin^2\varphi(\omega_0)\right]. \tag{16}$$

In the same manner, the output power of the second harmonic at $2f_0 = \omega_0/\pi$ is deduced up to the second order by combining (7) and (8) as follows:

$$P^2(\omega_0) = \frac{P^2_{\rm max}(\omega_0)}{4}\left\{1+k^4(\omega_0)+2k^2(\omega_0)\cos\left(2\varphi(\omega_0)\right)\right\} \tag{17}$$

and is found to be identical, up to the second order, to the output power of the second harmonic before bias compensation [see (12)].

B. Simulation Results and Discussion

In the previous section, we showed that selecting the appropriate transistor gate–source bias enables the output power of

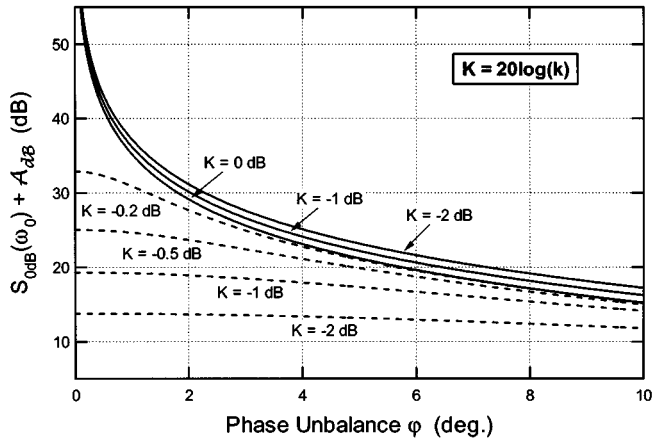

Fig. 5. Fundamental-frequency rejection evolution with phase and amplitude unbalance of the hybrid: (- - -) before bias compensation and (—) after bias compensation.

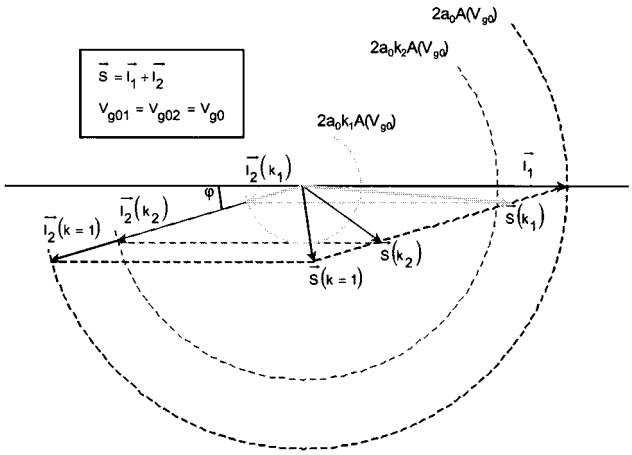

Fig. 6. Vectorial representation of the balanced active doubler output current at the fundamental frequency under standard operation: $V_{g01} = V_{g02}$.

the fundamental frequency to be minimized without changing, up to the second order, the output power of the second harmonic.

Assuming for instance that V_{g02} is fixed at near the pinchoff voltage of the transistor to maximize second harmonic generation [8]–[10], the optimum value for V_{g01} is deduced from (14)

$$V_{g01}(\omega_0) = k(\omega_0)\frac{A(V_{g02})}{A_2}\cos\varphi(\omega_0) - \frac{A_1}{2A_2}. \qquad (18)$$

In other words, this means that, at a given frequency f_0, tuning of the transistor gate–source bias according to (18) enables us to partially overcome the amplitude unbalance $k(\omega_0)$ and a phase unbalance $\varphi(\omega_0)$ of the hybrid. Consequently, the frequency at which the maximum fundamental-frequency rejection is achieved can be centered on f_0 instead of f_c when the transistors are symmetrically biased. This constitutes the concept of frequency tuning of balanced active doubler.

According to (16), perfect fundamental-frequency rejection is achieved if the hybrid's phase is perfectly balanced, regardless of amplitude unbalance. As shown in Fig. 5, after bias compensation, the fundamental-frequency rejection is improved and becomes mainly dependent on the phase unbalance of the hybrid. The strong degradation due to the amplitude unbalance (see also Fig. 3) is eliminated. On the contrary, the fundamental-frequency rejection increases in proportion to the amplitude unbalance expressed in decibels.

C. Graphical Interpretation of Bias Compensation Effect

The concept of bias compensation and, more particularly, the dependence of the fundamental-frequency rejection on the amplitude unbalance of the hybrid can be more easily understood by vectorial representation of the currents in the active doubler.

In standard operation where the transistors are identically biased ($V_{g01} = V_{g02} = V_{g0}$), the fundamental component of the output current of each transistor can be deduced from (3) and (4) as follows:

$$\begin{aligned} I_1(t) &= 2a_0\mathcal{A}(V_{g0})\cos(\omega_0 t) \\ I_2(t) &= 2a_0k(\omega_0)\mathcal{A}(V_{g0})\cos\left(\omega_0 t + 180^\circ + \varphi(\omega_0)\right). \end{aligned} \qquad (19)$$

Fig. 6 shows the vectorial representation of the current components in a time-dependant coordinate system for different values of amplitude unbalance and a fixed value of the phase unbalance. When the amplitude unbalance induced by the hybrid is more important, that is to say, the k factor decreases ($k < 1$, $k \searrow$), the modulus of $\overrightarrow{I_2}$ decreases, whereas $\overrightarrow{I_1}$ remains unchanged. Therefore, as shown in Fig. 6, the modulus of the addition $\overrightarrow{S}$ of these two vectors forming the total output current of the fundamental frequency of the doubler is increased. Consequently, the fundamental-frequency rejection decreases when the amplitude unbalance of the hybrid becomes more important (see Fig. 3).

Let us now consider the bias compensation concept. Assuming that V_{g02} is fixed and that V_{g01} is given by (18), the fundamental component of the output current of each transistor [see (3) and (4)] is given by

$$\begin{aligned} I_1(t) &= 2a_0k(\omega_0)\mathcal{A}(V_{g02})\cos(\omega_0 t)\cos\varphi(\omega_0) \\ &= a_0k(\omega_0)\mathcal{A}(V_{g02}) \\ &\quad \cdot\left[\cos\left(\omega_0 t + \varphi(\omega_0)\right) + \cos\left(\omega_0 t - \varphi(\omega_0)\right)\right] \\ I_2(t) &= 2a_0k(\omega_0)\mathcal{A}(V_{g02})\cos\left(\omega_0 t + 180^\circ + \varphi(\omega_0)\right). \end{aligned} \qquad (20)$$

The vectorial representation of these current components is shown in Fig. 7 for a different value of the amplitude unbalance and a fixed value of the phase unbalance. When the amplitude unbalance induced by the hybrid is more important ($k < 1$, $k \searrow$), both the module of the $\overrightarrow{I_1}$ and $\overrightarrow{I_2}$ vectors decrease in the same manner. Therefore, as shown in Fig. 7, the modulus of the result $\overrightarrow{S}$ of these two vectors decreases. Consequently, the fundamental-frequency rejection increases when the amplitude unbalance of the hybrid becomes more important. This explains the behavior of the fundamental-frequency rejection in Fig. 5.

D. Limits of the Concept

The first limit to the frequency-tuning concept lies in the existence of the transistor dc-bias voltages that compensate for the hybrid's asymmetry. A consideration of the transistor behavior when biased near the pinchoff voltage lets us assume that term A_1/A_2 is small. Moreover, even for a phase unbalance of approximately 10°, $\cos\varphi$ remains close to unity. Therefore, the difference $\delta V = V_{g01} - V_{g02}$ between the two bias voltages is

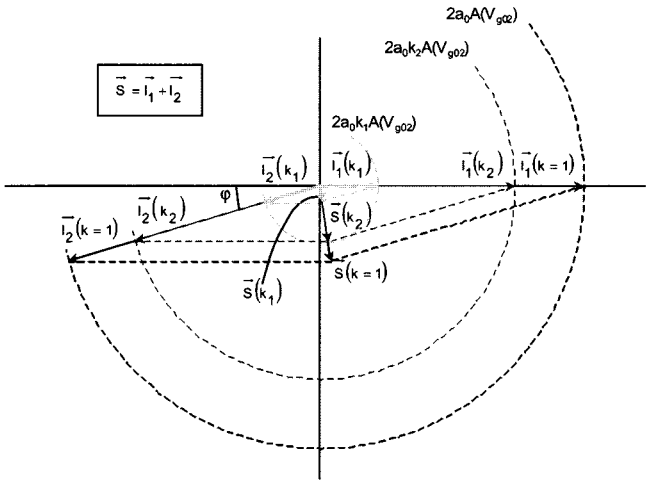

Fig. 7. Vectorial representation of the balanced active doubler output current at the fundamental frequency with bias compensation: $V_{g01} = V_{g02}k\cos\varphi - (A_1/2A_2)(1 - k\cos\varphi)$.

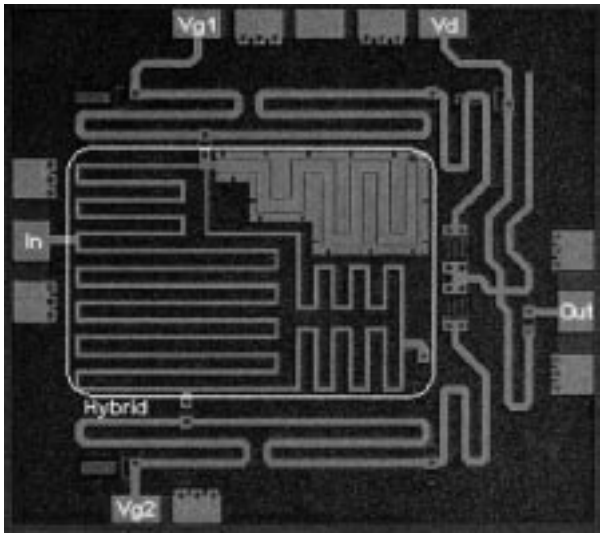

Fig. 8. Microphotograph of the active V-band balanced frequency doubler. Intrinsic size of the doubler is 1 mm^2.

expected to remain small and realizable for small values of hybrid phase and amplitude unbalance.

When the difference between the two transistor bias voltages becomes significant, the same Taylor series representation cannot be used for the two transistors and our analysis is only approximate.

The second limit to the proposed concept lies in the phase balance performance of the hybrid. Indeed, as shown in Fig. 5, the bias compensation concept eliminates the strong degradation in fundamental-frequency rejection caused by the amplitude unbalance of the hybrid. However, the fundamental-frequency rejection remains highly dependent on the phase unbalance. For $\pm 1.5^\circ$ phase unbalance and -2 dB amplitude unbalance, the improvement in the fundamental-frequency rejection due to bias compensation is approximately 20 dB, but this falls to 14.1 dB (8.7 dB) for $\pm 3^\circ$ ($\pm 6^\circ$) phase unbalance. This determines the bandwidth over which the doubler can achieve high fundamental-frequency rejection. Moreover, this result shows that, considering the bias compensation concept, future improvements in the hybrid performance should mainly concentrate on improving the phase characteristics.

IV. Overview of the MMIC Design

The proposed concept is experimentally validated using a previously fabricated V-band pHEMT frequency doubler [5] whose design is quickly overviewed here.

Fig. 8 presents a microphotograph of the doubler. The novel rat-race hybrid reported in [6] is used to achieve high spectral purity and broad-band operation. This hybrid exhibits a power dividing balance of better than 1.1 dB and a phase balance of better than 2° from 28.8 to 39.4 GHz. The transistors used are 0.15-μm long and 220-μm (50 μm $\times$ 4) wide Panasonic pHEMTs [13]. Table I details the doubler performance measured in standard operation ($V_{g01} = V_{g02}$).

TABLE I
Summary of Measured Doubler Performance

Input Power	14 dBm
Highest Fundamental frequency Rejection	48 dB at f_0=32.5 GHz
Highest Isolation	40 dB at f_0=32.5 GHz
Conversion Gain	-8.5 dB at f_0=32.5 GHz
Bandwidth for Isolation >30 dB	31.7 ~ 36 GHz
Bandwidth for Fundamental Rejection >35 dB	31.5 ~ 37.5 GHz

V. Experimental Results

A. Validation of the Frequency Tuning Concept

The measurements were performed under the same conditions reported in [5]: the drain voltage was 2 V and the input power was 14 dBm for minimum conversion loss and before the saturation of the second harmonic. The gate–source bias voltage of the second transistor V_{g02} (see Fig. 1) was fixed to -0.7 V, i.e., near the threshold voltage, to maximize the generation of the second harmonic.

The dotted line traces in Figs. 9 and 10 indicate the results gained when the transistors were identically biased: $V_{g01} = V_{g02} = -0.7$ V.

The annotated traces a–h in Figs. 9 and 10 refer to different bias level of the first transistor V_{g01} (see Fig. 1). Setting $\delta V = V_{g01} - V_{g02}$, the correspondence is a: $\delta V = -0.33$ V, b: $\delta V = -0.29$ V, c: $\delta V = -0.22$ V, d: $\delta V = -0.14$ V, e: $\delta V = -0.1$ V, f: $\delta V = -0.04$ V, g: $\delta V = -0.05$ V, h: $\delta V = -0.028$ V.

Fig. 9 shows the measured output power of the fundamental frequency and the second harmonic in the cases just described. The voltage difference δV set for measurements a–h was optimized so that a minimum of the output power of the fundamental harmonic is achieved from 27 to 36 GHz with a regular step of 1 GHz. As expected, this difference δV remained small and realizable over a large range of frequencies. Bellow 27 GHz, δV becomes too important and the bias compensation process is inefficient, leading to a strong decrease in the second harmonic output power and inefficient rejection of the fundamental frequency. This limitation of the frequency-tuning concept can also be imputed to the input and output matching circuits that

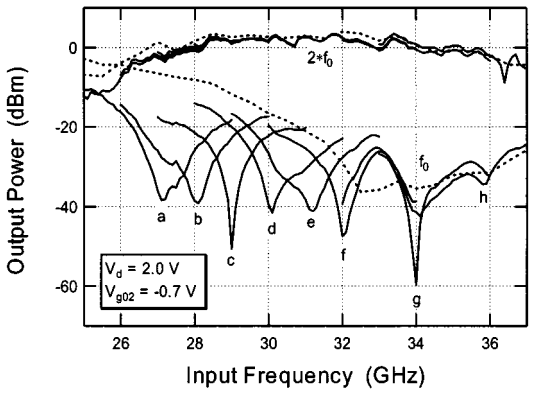

Fig. 9. Output power of the fundamental frequency and the second harmonic versus frequency at different transistor bias unbalance values. The dotted traces indicate the output powers when the transistors are identically biased.

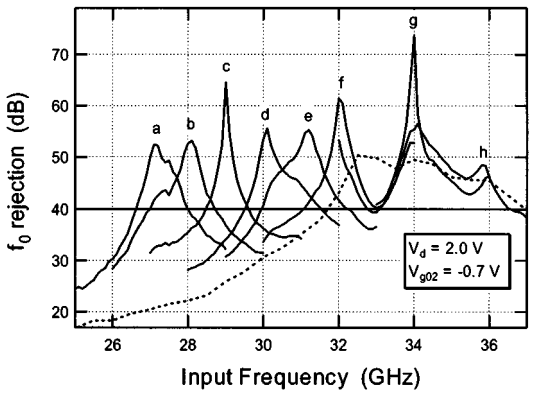

Fig. 10. Fundamental-frequency rejection versus the input frequency for different transistor bias unbalance values. The dotted trace indicates the fundamental-frequency rejection when the transistors are identically biased.

are limited in frequency and design to allow operation of each transistor near the threshold voltage.

In the frequency band from 32.5 GHz to approximately 36 GHz, corresponding to the minimum phase and amplitude unbalance of the hybrid, the bias difference δV between the two transistors is so small that control of the bias voltages is difficult. Therefore, the bias compensation process is not clearly demonstrated at 33 and 35 GHz. However, this frequency band already corresponds to the best performance of the frequency doubler in standard operation ($V_{g01} = V_{g02}$), where the bias compensation process is not needed. Above 36 GHz, the input and output matching circuits very probably limit the effectiveness of bias compensation.

Since bias compensation of the hybrid's asymmetry is optimized at one frequency, it quickly becomes inefficient at a different frequency and optimization must be performed again. Therefore, traces a–h of Figs. 9 and 10 are much sharper than the standard operation trace.

Fig. 10 shows the measured fundamental-frequency rejection of the balanced active doubler. A comparison to the fundamental-frequency rejection measured under standard operation (dotted-line trace) shows that the concept of frequency tuning substantially improves the usable bandwidth of the balanced doubler while still achieving high fundamental-frequency rejection. Local fundamental-frequency rejection better than 40 dB

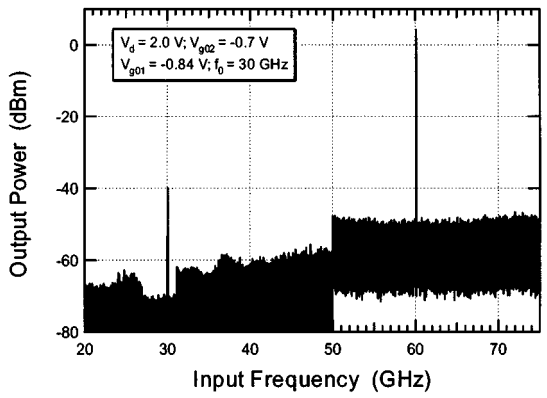

Fig. 11. Spectrum measurement of the balanced frequency doubler under bias compensation at $\delta V = -0.14$ V with input signal frequency $f_0 = 30$ GHz (case d in Fig. 9).

is achieved from 26.7 to 37 GHz. As regards the measured fundamental-frequency rejection in standard operation, this performance represents an expansion of the usable bandwidth of over 100%.

Also as expected, Fig. 9 shows that the output power of the second harmonic is slightly affected by the gate–source bias asymmetry of the transistors. Consequently, the isolation between the fundamental frequency and second harmonic is also substantially improved by bias compensation. Local isolation higher than 30 dB is achieved from 26.9 to 36 GHz. As regards isolation measured under standard operation, this represents an expansion of the usable bandwidth of over 100%.

B. Spectral Measurements

Fig. 11 shows the spectrum measurement of the frequency doubler operating with asymmetrically biased transistors $\delta V = -0.14$ V, which corresponds to the optimum bias unbalance in terms of achieving maximum fundamental-frequency rejection at 30 GHz.

The difference in noise level is due to a change of the measurement system at 50 GHz. The noise floor for the second harmonic is more than 50 dB under the desired signal.

Fig. 11 and the spectrum measurements done under the other cases, i.e., a–h of Fig. 9, confirm that no undesired spurious signal is generated when the transistors are asymmetrically biased. This confirms that the concept of frequency tuning is particularly suited to the realization of widely tunable and high spectral purity V-band frequency sources.

VI. Conclusion

An analysis of balanced active frequency doubler has been introduced to clarify the fundamental-frequency rejection performance of such devices. From this analysis, we propose the new concept of frequency tuning as a very simple and very effective way to extend the usable bandwidth of balanced active doublers. This concept is validated on a previously fabricated V-band pHEMT frequency doubler. Improvement of the usable bandwidth in terms of spectral purity (fundamental-frequency rejection $>$ 40 dB and isolation $>$ 30 dB) is over 100%.

Therefore, we can conclude that the proposed concept is particularly well suited to the realization of widely tunable and high spectral purity V-band frequency sources.

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Belinda Piernas was born in Sete, France, in 1972. She graduated from the Institut Supérieur d'Electronique du Nord, Lille, France, in 1995, and received the Ph.D. degree from the Institut National des Sciences Appliquées de Rennes, Rennes, France, in 1999.

In 1995, she joined the Optoelectronic Laboratory, Institut Supérieur d'Electronique de Bretagne, Brest, France, where she was engaged in the design and fabrication of an opto-electronic self-routing cell-switch. Her activity also included the design and fabrication of high-speed opto-electronic integrated circuits based on vertical cavity surface emitting lasers (VCSELs), MMICs, and optical interconnections. Since 1999, she has been with the NTT Network Innovation Laboratories, Yokosuka, Japan, where she is engaged in the design of wireless communication integrated circuits for the future high-speed communication systems using 3-D MMIC technology. Her current interest concerns the design of millimeter-wave single-chip transceivers, including all the functionality of the receiver and the transceiver block up to the antennas.

Dr. Piernas was the recipient of the 2001 Young Engineer Award presented by the Institution of Electrical Engineers of Japan.

Kenjiro Nishikawa (A'93–M'99) was born in Nara, Japan, in 1965. He received the B.E. and M.E. degrees in welding engineering from Osaka University, Suita, Japan, in 1989 and 1991, respectively.

In 1991, he joined the NTT Radio Communication Systems Laboratories (now the NTT Network Innovation Laboratories), Yokosuka, Japan, where he has been engaged in research and development of 3-D and uniplanar MMICs on Si and GaAs and their applications. He is currently interested in millimeter-wave communication systems and microwave/millimeter-wave photonics communication systems.

Mr. Nishikawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1996 Young Engineer Award presented by the IEICE.

Tadao Nakagawa (M'91) received the B.E. and M.E. degrees in material physics and the Dr.Eng. degree in communication engineering from Osaka University, Osaka, Japan, in 1986, 1988, and 1997, respectively.

In 1988, he joined the NTT Radio Communication Systems Laboratories, Yokosuka, Japan, where he was engaged in research and development of MMICs and microwave synthesizers. From 1997 to 1999, he was an Associate Manager with the STE Telecommunication Engineering Company Ltd., where he served as a Technical Consultant on wireless communications to the Seiko Epson Corporation, Nagano, Japan. Since 1999, he has been a Senior Research Engineer at the NTT Network Innovation Laboratories, Yokosuka, Japan, where he is currently involved in the design of millimeter-wave transceivers and multiband transceivers.

Dr. Nakagawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1995 Young Engineer Award presented by the IEICE.

Hitoshi Hayashi (M'94) received the B.Eng., M.Eng., and Ph.D. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 1990, 1992, and 2000, respectively.

In 1992, he joined the NTT Radio Communication Systems Laboratories, Yokosuka, Japan. He is currently with the NTT Network Innovation Laboratories, Yokosuka, Japan, where he is engaged in the development of wireless communication systems. Since September 2000, he has been involved in wireless systems research at the Massachusetts Institute of Technology (MIT), Cambridge, as a Visiting Scientist.

Dr. Hayashi is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1998 Young Engineer Award presented by the IEICE.

Katsuhiko Araki received the B.E. and M.E. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1979 and 1981, respectively.

In 1981, he joined the NTT Electrical Communications Laboratories, Yokosuka, Japan, where he has been engaged in research on GaAs monolithic microwave circuits and in the development of communication satellite on-board transponders. He is currently the Senior Research Engineer, Supervisor, at the NTT Network Innovation Laboratories, Yokosuka, Japan.

Mr. Araki is a member of the American Institute of Aeronautics and Astronautics (AIAA) and the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1988 Sinohara Prize presented by the IEICE.